	Abbreviation	Description
A	A0–A15	Address I/O
	AC	All Clear
	ACKDTREQ	Used for Two Way Communication
	ADC0–7	AD Chroma 0–7
	ADCLK	AD Clock
	A/DB-Y	A/D Conv. B-Y
	A/DR-Y	A/D Conv. R-Y
	A/DY	A/D Conv. Y
	AVDD	Analog Power Source
	AVSS	Analog GND
	ADY0–7	AD Y 0–7
B	B	Blue
	BEO	Print (H)
	BFP	Burst Flag Pulse
	BGP POSI	Burst Gate Pulse Position
	BGP WIDTH	Burst Gate Pulse Width
	BLNK	Letter Back Ground Output
	B PEAK	Video Black Peak
	BUS INH	Bus Release Signal
C	CAS	Column Address Strobe
	CAS 0S, 1S, 2S, 3S	Cassette Detection 0S, 1S, 2S, 3S
	CASL	Cassette Detection L
	CASI/MODB	Cassette In Detection/Mode Sensor B
	CG-SYNC	Character Generator Sync
	C-IN	Chroma Input
	CLK RGB	DA Clock RGB
	COMP	Comparator
	C OUT	Chroma Output
	CPS	Composite Signal
	CRTSW, CRTSW1	Ink Cassette Detection (EX 1st H/Non L)
	CRT/PHLD	Ink Cassette, Paper Switch
	CS	Chip Select
	CS	Input Current Soft Start Capacity
	C-SYNC	Component Sync
	CT	Oscillation Time Constant
D	D0–D7	Data Output
	DO0–7	Microprocessor Data Bus 0–7
	DAB0–7	Digital Bule 0–7
	DAR0–7	Digital Red 0–7
	DAY0–7	Digital Y 0–7
	D/A B-Y	DA Conv. B-Y
	D/A R-Y	DA Conv. R-Y
	D/A Y	DA Conv. Y
	DA CLK	Digital Conv. Clock
	DB1–8	Digital Blue 1–8
	DR1–8	Digital Red 1–8
	DG1–8	Digital Y 1–8
	DCA	Decoder Input A
	DCB	Decoder Input B
	DCSB	DSP CP Select Input
	DEW	Dew Condensation Detection H
	DGO	Thermal Head Enable Output

	Abbreviation	Description
D	DGCK	Data Latch Clock Input
	DGIN	Digital Memory Data Input
	DIPSW0–5	Dip Switch 0–5
	DM	Digital Memory
	DMA	Direct Memory Access
	D MA0–8	Digital Memory Address
	DMCAS	Digital Memory Column Address Strobe
	DMWE	Digital Memory Write Enable
	DMOE	Digital Memory Output Enable
	DRWB	DSP Read/Write Input
	DS	Output Data Select L
	DSP	Digital Signal Processor
	DTAVAIL	Used for Two way Communication
	DVDD	Digital Power Source
	DVSS	Digital GND
E	ERR LED	Error LED
	EXO-	External Input
	EXRM	L at External Memory
F	F270	System Clock 27MHz
	FAN MOTOR ON H	FAN MOTOR ON: H
	FAN 0, 1	Fan Motor Drive 0, 1
	FAN–V	Fan Motor Power Source
	FB	Feed Back
	FB CAP	Feed Back Capacity
	F DFL, FD/FL	Field: H/Frame: L
	FIL 0–1	Filter Control 0, 1
	FNM	Fan Motor ON H
	FSC	Sub Carrier Frequency
	FSC 180 OUT	Sub Carrier 180° Output
	F SEL	ODD Field/EVEN Field Select
G	G	Output Enable Input
	GMA 0–8	Video Memory Address
	GMD 10–27	Video Memory Data
	GMCAS	VIdeo Memory Column Address Strobe
	GMDEN	Video Memory Output Enable
	GMRAS	Video Memory Row Address Strobe
	GMS CK	Print Counter Clock
	GMWEN	Video Memory Write Enable
H	HDM 0, HDM 1	Head Motor Drive Pulse
	HDP	H Drive Pulse
	HEAD A, B	Head Motor Position Detection
	HSIN, O	H Sync In, Out
	HSKO	Serial Clock Output
	HOR	Horizontal Sync
	HOSTCLK	Data Clock
	H SEL	HD Select Write: H/Read: L